ABSTRACT

There are provided a reference voltage generating method used for reading out operation of a memory cell having amplification ability, and a dummy cell. The memory cell is comprised of a read NMOS transistor, a write transistor, and a coupled-capacitance. The dummy cell is made such that two memory cells are connected in series. The dummy cell is arranged at the most far end of each of the data lines against the sense amplifier. A reference voltage is generated by making a difference in an amount of current flowing in each of the read NMOS transistors of the memory cell and the dummy cell. As a result, DRAM showing a higher speed, a higher integrated and a lower electrical power as compared with those of the prior art device can be realized.